UTILITY PATENT APPLICATION TRANSMITTAL LETTER

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
WN-2205

To the Assistant Commissioner for Patents:

Transmitted herewith for filing is the patent application of:
Masamoto TAGO and Akihiro DOHYA
corresponding to Japanese application 193962/1999, filed July 8, 1999,
entitled: SYSTEM SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Enclosed are:

X	21 pages of specification.
X	14 sheets of formal drawings.
X	a newly-executed declaration of the inventors.
	a copy of an executed declaration of the inventor from prior application Serial No. , filed .
	incorporation by reference. The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied as indicated in the preceding box, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
X	an assignment of the invention to NEC CORPORATION, including assignment cover sheet.
	Information Disclosure Statement with Form PTO-1449.
	copies of the Information Disclosure Statement citations.
	preliminary amendment.
X	return receipt postcard (MPEP 503), specifically itemized.
	a verified statement to establish small entity status under 37 CFR 1.9 and 1.27.
	a verified statement to establish small entity status filed in prior application. Status is still proper and desired.
X	a certified copy of the Japanese Priority Document.
X	other: inventor information sheet.

If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information.*

[] Continuation [] Divisional [] Continuation-in-part (CIP)

of prior application No. , filed .

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UTILITY PATENT APPLICATION TRANSMITTAL LETTER (continued)	Docket No. WN-2205

CLAIMS AS FILED

	NO. FILED	NO. EXTRA	RATE	FEE
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INDEPENDENT CLAIMS	2 - 3 =	0	x$ 78	0
MULTIPLE DEPENDENT CLAIM PRESENT			$ 260	
			TOTAL	$ 726
If applicant has small entity status under 37 CFR 1.9 and 1.27, then divide total fee by 2, and enter amount here.			**SMALL ENTITY TOTAL**	$

X	A check in the amount of $766 to cover the filing fee is enclosed.
X	The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to Deposit Account No. 25-0120 in the name of Young & Thompson, as described below. A duplicate copy of this sheet is enclosed.
	Charge the amount of $ as filing fee.
X	Credit any overpayment.
X	Charge any additional fee required under 37 CFR 1.16 and 1.17, during the pendency of this application.
	Charge the issue fee set in 37 CFR 1.18 at the mailing of the Notice of Allowance.

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APPLICATION INFORMATION

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Title Line Two::	OF MANUFACTURING THE SAME
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Formal Drawings?::	YES
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SYSTEM SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Background of the Invention:

This invention relates to a system semiconductor device and a method of manufacturing the same, and in particular, to a system semiconductor device having a plurality of functional blocks.

The conventional system LSI (Large-Scale-Integrated circuit) generally includes a plurality of functional blocks. Herein, it is to be noted that the functional block serves as a circuit unit for realizing a specific function. In such a system LSI, complex functions are integrated on one chip.

The conventional method of manufacturing the system LSI has been carried out as follows.

A plurality of functional blocks are first fabricated on a silicon chip. Thereafter, a circuit wiring layer which electrically connects the functional blocks to each other is formed on the silicon chip by the use of a metal vaporizing method or a metal plating method.

Subsequently, an insulating film is formed thereon and the circuit wiring layer and the insulating layer are sequentially laminated. Thereby, a global wiring layer serving as a multi-wiring layer is formed on the silicon chip.

Thus, a plurality of circuit wiring layers and insulating layers conventionally has been laminated for many times to manufacture the system LSI.

However, the conventional system LSI has the following problems.

First, manufacturing yield is degraded. This reason will be explained below. Namely, an external stress is applied or stress-migration occurs because a plurality of circuit wiring layers and insulating layers are laminated.

Under this circumstance, the circuit wiring layer is peeled from the insulating layer. Consequently, a physical strength is inevitably lowered.

Further, an electrical connection between layers is damaged. In consequence, electrical connection reliability is readily degraded.

Second, a manufacturing duration becomes long. This reason will be explained as follows.

Namely, after the system LSI is fabricated, a plurality circuit wiring layers and insulating layers are alternately laminated on a system LSI cell. To this end, complex and many steps are inevitably required.

Third, selection degree of freedom concerning materials of the global wiring layer and manufacturing processes is lowered. This reason will be described below.

That is, the manufacturing process of the global wiring layer or the materials of the circuit wiring layers and the insulating layers are restricted in dependency upon a laminating process. Consequently, the manufacturing process and the material can not freely or suitably selected.

Fourth, physical characteristics and electrical characteristics are degraded, and the manufacturing cost becomes high. This reason will be explained as follows.

The manufacturing process of the global wiring line layer or the materials of the circuit wiring layers and the insulating layers are restricted in accordance with the laminating process. Consequently, the manufacturing process and the material can not freely or suitably selected.

Fifth, the electrical characteristic for a high-frequency signal is degraded. This reason will be explained below.

That is, a system LSI cell portion and the global wiring line layer are adjacently arranged to each other. In consequence, dielectric constants are enhanced to each other, and impedance of the circuit is also increased.

Summary of the Invention:

It is therefore an object of this invention to provide a system semiconductor device which has a simple manufacturing step and a cheap manufacturing cost.

It is another object of this invention to provide a system semiconductor device which is capable of improving physical and electrical characteristics.

According to this invention, a system semiconductor device has a system LSI cell portion and a global wiring layer.

The system LSI cell portion includes a plurality of functional blocks for realizing specific functions. In this event, each of the functional blocks serves as a unit circuit and is arranged on a semiconductor chip.

A global wiring layer has a wiring layer on a semiconductor substrate.

With this structure, the system LSI cell portion is laminated or combined with the global wiring layer such that the functional blocks are electrically connected to each other.

In this case, a plurality of the system LSI cell portions are formed on a semiconductor wafer while a plurality of the global wiring layers are formed on the semiconductor substrate.

In this condition, the semiconductor wafer and the semiconductor substrate are laminated, diced and separated to obtain a plurality of the system semiconductor devices.

The global wiring layer includes a first wiring layer formed on the semiconductor substrate, an insulating layer formed on the first wiring layer, and a second wiring layer and an adhesive layer formed on the insulating

layer.

Alternatively, the global wiring layer may include a first wiring layer formed on an organic substrate, an insulating layer formed on the first wiring layer, and a second wiring layer and an adhesive layer formed on the insulating layer.

Instead, the global wiring layer may have a first wiring layer formed on the semiconductor substrate, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer, and inner bumps formed on the second wiring layer.

Alternatively, the global wiring layer may comprise a first wiring layer formed on an organic substrate, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer, and inner bumps formed on the second wiring layer.

In this case, the insulating layer preferably includes a via which electrically connects the first wiring layer with the second wiring layer.

The global wiring layer may have bumps for electrically connecting to an external circuit on a surface thereof.

Further, the global wiring layer may include buried vias which electrically connect the functional blocks to an external circuit.

Moreover, the global wiring layer may have at least one or more of the wiring layers.

In addition, the global wiring layer may have at least one or more of the insulating layers.

<u>Brief Description of the Drawings</u>:

Fig. 1A is a plan view showing a system LSI according to a first embodiment of this invention;

Fig. 1B is a cross sectional view, taken along I-I line in Fig. 1A;

Fig. 2A is a plan view showing a system LSI cell portion according to a first embodiment of this invention;

Fig. 2B is a cross sectional view, taken along II-II line in Fig. 2A;

Fig. 3A is a plan view showing a global wiring layer according to a first embodiment of this invention;

Fig. 3B is a cross sectional view, taken along III-III line in Fig. 3A;

Figs. 4A through 4C are cross sectional views showing a method of manufacturing a system LSI cell portion of a system LSI according to a first embodiment of this invention;

Figs. 5A through 5F are cross sectional views showing a method of manufacturing a global wiring layer of a system LSI according to a first embodiment of this invention;

Figs. 6A through 6C are cross sectional views showing a method of manufacturing a system LSI according to a first embodiment of this invention;

Fig. 7 is a plan view showing a system LSI according to a second embodiment of this invention;

Figs. 8A through 8E are cross sectional views showing a method of manufacturing a global wiring layer of a system LSI according to a second embodiment of this invention;

Figs. 9A through 9C are cross sectional views showing a method of manufacturing a system LSI according to a second embodiment of this invention;

Fig. 10 is a plan view showing a system LSI according to a third embodiment of this invention;

Figs. 11A through 11F are cross sectional views showing a method of manufacturing a global wiring layer of a system LSI according to a third embodiment of this invention;

Figs. 12A through 12C are cross sectional views showing a method of manufacturing a system LSI according to a third embodiment of this invention;

Fig. 13 is a plan view showing a system LSI according to a forth embodiment of this invention;

Figs. 14A through 14E are cross sectional views showing a method of manufacturing a global wiring layer of a system LSI according to a fourth embodiment of this invention;

Figs. 15A through 15C are cross sectional views showing a method of manufacturing a system LSI according to a fourth embodiment of this invention; and

Figs. 16A through 16E are cross sectional views showing a method of manufacturing a system LSI according to a fifth embodiment of this invention;

Description of Preferred Embodiments:

(First embodiment)

Referring to Fig. 1 through Fig. 3, description will be made about a system LSI according to a first embodiment of this invention.

A system LSI illustrated in Fig. 1 is formed by laminating or combining a system LSI cell portion 7 illustrated in Fig. 2A with a global wiring layer 8 illustrated in Fig. 3B on the condition that the global wiring layer is turned over.

In this case, the system LSI cell portion 7 has functional blocks 2 to 6, as illustrated in Fig 2. While, the global wiring layer 8 mutually and electrically connects the functional blocks 2 to 6 formed on the system LSI cell portion 7, as illustrated in Fig. 3.

The system LSI cell portion 7 is composed of a silicon chip 1, and the functional blocks 2 to 6 formed on the surface of the silicon chip 1, as shown in Figs. 2A and 2B.

In this case, the silicon chip 1 is formed by processing and separating a variety of semiconductor wafers such as a silicon wafer by a dicing process. Although the silicon chip 1 is realized by the silicon, the

other arbitrary semiconductor materials may be used instead of the silicon.

Further, each of the functional blocks 2 to 6 serves as an unit circuit which realizes a specific function as a memory or a microcomputer, and is fabricated by performing a patterning process, an ion implanting process, and a stepper processing process for each part of the silicon chip 1, and has pads 2a to 6a serving as electrodes on the surface.

The global wiring layer 8 is composed of a silicon substrate 11, buried vias 12, a first wiring layer 13, an insulating layer 14, a second wiring layer 15, and an adhesive layer 16.

With such a structure, the global wiring line layer 8 mutually and electrically connects the functional blocks 2 to 6 on the system LSI cell portion 7, and is electrically coupled to an external circuit.

Herein, it is to be noted that the silicon substrate 11 is formed by processing and separating a variety of semiconductor wafers such as the silicon wafer by the use of the dicing process.

The buried via 12 is formed by performing a buried process for an internal of the silicon substrate 11 to penetrate the internal of the silicon substrate 11, and is formed by conductive material which electrically connects the functional blocks 2 to 6 with the external circuit.

In this event, the buried via 12 is formed by the use of a selection CVD (Chemical Vapor Deposition) method, a metal plating method or a conductive paste method.

The first wiring layer 13 is deposited by shaping conductive material of a variety of metals such as copper to a specific pattern on the surface of the silicon substrate 11, and electrically connects the buried via with a via 14a.

Herein, it is to be noted that the metal film serving as the first wiring layer 13 is formed by the use of the plating method or the sputtering method.

The insulating layer 14 is formed by depositing insulating material on the surface of the first wiring layer 13, and electrically insulates the first wiring layer 13 from the second wiring layer 15.

In this case, silicon compound of SiOx or SiNx, organic material ,such as, polyimide and compound fluoride may be used as the insulating material of the insulating layer 14.

The via 14, which electrically connects the first wiring layer 13 with the second wiring layer 15, is formed at a specific position of the insulating film 14 by the use of the selective CVD method, the metal plating method or the conductive paste method. Herein, copper or copper alloy may be used as the material of the via 14.

The second wiring layer 15 is deposited by shaping conductive material of a variety of metals to a specific pattern on the surface of the insulating layer 14, and electrically connects the via 14a with electrodes 2 to 6 of the functional blocks 2 to 6.

Herein, it is to be noted that the metal film serving as the second wiring layer 15 is formed by the use of the plating method or the sputtering method.

The adhesive layer 16 is formed by a variety of adhesive materials, such as, heat-hardening resin or light-hardening resin, and is formed on the surface of the second insulating layer 15.

Although the first and second wiring layers 13 and 15 of the global wiring layer 8 are formed by Al, Al alloy, Cu, and Cu alloy, arbitrary conductive materials may be used other than them.

Similarly, although the insulating layer 14 is formed by a silicon oxide film, a silicon nitride film, and polyimide, optional material may be used other than them.

Likely, the buried via 12 and the via 14a are formed by burying the conductive metal for internal surface of the buried via 12 and the via 14a by

the use of the selective CVD method or by plating the conductive metal, such as, Cu.

Alternatively, the buried via 12 and the via 14a may be formed by filling and hardening the conductive paste mixed with metal powder inside the buried via 12 and the via 14a. Instead, they may be formed by using an arbitrary method by the use of an optional conductive material.

Subsequently, description will be made about a method of manufacturing the system LSI according to the first embodiment.

Referring to Figs. 4A through 4C, description will be made about a method of manufacturing the system LSI cell portion 7 of the system LSI 10.

First, the silicon chip 1 is prepared by dicing and separating a silicon wafer, as illustrated in Fig. 4A.

Next, the pattern forming process, the ion injection process and the stepper process are carried out for the silicon chip 1 to form the functional blocks 2 to 6 on the silicon chip 1, as illustrated in Fig. 4B.

Herein, the respective gates in the functional blocks 2 to 6 are connected to each other by the use of polysilicon or a aluminum wiring pattern which is used in the general structure of the LSI wiring layer.

Subsequently, external terminals are formed to connect between the respective functional blocks 2 to 6. To this end, pads 2a to 6a are formed at specific portions on the surface of the functional blocks 2 to 6, as illustrated in Fig. 4C.

In this event, the connection net number between the functional blocks 2 to 6 of the pads 2a to 6a is largely low in comparison with the connection net number in the functional blocks 2 to 6. Consequently, the number of the pads 2a to 6a may be not much high.

Therefore, if each of the pads 2a to 6a has a size of 10 μ m and a space (pitch) of 12 μ m between the pads 2a to 6a, the pads 2a to 6a can be formed with such number that enough connection is possible.

Meanwhile, it is to be noted that each of the pads 2a to 6a may be formed by the use of metal film, such as, copper, gold, gold tin solder, tin lead solder. Thus, the system LSI cell portion 7 is completed.

Referring to Figs. 5A through 5F, description will be made about the global wiring layer 8 of the system LSI 10.

First, the silicon substrate 11 is prepared, as illustrated in Fig. 5A.

Next, the buried vias 12 are formed inside the silicon substrate 11 by the use of the selective CVD method or the metal plating method, as illustrated in Fig. 5B.

Successively, the conductive material, such as, Cu is deposited on the surface of the silicon substrate 11, and the first wiring layer 13 is formed by a patterning process after an exposing and developing process, as shown in Fig. 5C.

Subsequently, the insulating film 14 is deposited on the surface of the first wiring layer 13. Thereafter, the vias 14 are formed at specific portions in the insulating layer 14 so as to penetrate the insulating layer 14, as shown in Fig. 5D. Thereby, the via 14a electrically mutually connects the first wiring layer 13 with the second wiring layer 15.

Next, the conductive material, such as, Cu and Au is deposited on the surface of the insulating layer 14 and the vias 14a by the sputtering method or the plating method, and the second wiring layer 15 is formed by the patterning process after the exposing and developing process, as illustrated in Fig. 5E.

Finally, heat-hardening adhesives are supplied to a region except for a region where the second wiring layer 15 is formed on the surface of the global wiring layer 8 to form the adhesive layer 16, as illustrated in Fig. 5F. Thus, the global wiring layer 8 is completed.

In the first embodiment, the following process rule may be, for example, adopted.

Namely, a line width is equal 10 μ m, and a wiring space is equal to 10 μ m. Further, a conductor thickness of the first and second wiring layer 13 and 15 is equal to 10 μ m while an insulating thickness of the insulating layer 14 is equal to 10 μ m.

Thus, the global wiring layer 8 can be formed by the use of a relatively rough process rule in the first embodiment. Consequently, only the global wiring layer 8 can be independently manufactured by using cheaper equipment than a mounting equipment for forming the system LSI cell portion 7.

Although the first and second wiring layers 13 and 15 and the insulating layer 14 are used as the global wiring layer, the layer number of these wiring layers and the insulating layer is not restricted, and a single layer or a multiple layer may be used.

Referring to Figs. 6A through 6C, description will be made about a method of manufacturing the system LSI 10.

The global wiring layer 8 is transferred onto the system LSI cell portion 7, as illustrated in Fig. 6A. In this event, the system LSI cell portion 7 is mounted on a stage (not shown) while the global wiring layer 8 is transferred on the condition that the global wiring layer 8 is turned over.

Under this circumstance, the pads 2a to 6a of the system LSI cell portion 7 are positioned in opposition to the second wiring layer 15 of the global wiring layer 8 by using a position detecting device, such as, an image camera.

Next, the LSI cell portion 7 and the global wiring layer are overlapped to each other. In the condition, a pressure is applied upwards and downward, and a heating process is carried out.

Thereby, the adhesive layer 16 is heat-hardened, and the system LSI cell portion 7 and the global wiring layer 8 are bonded and hardened. Consequently, the pads 2a to 6a of the system LSI cell portion 7 are

coupled with the second wiring layer 15 of the global wiring layer 8, and are mutually and electrically connected, as illustrated in Fig. 6B.

Finally, the silicon substrate 11 is polished from an upper side of the global wiring layer 8, as illustrated in Fig. 6C. Thereby, the buried vias 12 are exposed on the surface, and serves as the electrodes for the external circuit. Thus, the system LSI 10 is completed.

Thus, after the system LSI cell portion 7 and the global wiring layer 8 are independently manufactured, and they are laminated or combined to form the system LSI 10, in the first embodiment.

After the system LSI cell portion 7 and the global wiring layer 8 are laminated or combined to each other, the buried vias 12 are exposed to the surface in the first embodiment.

Alternatively, after the buried vias 12 are exposed to the surface before the laminating or combining step, the system LSI may be manufactured by laminating or combining them.

(Second Embodiment)

Referring to Fig. 7, description will be made about a system LSI according to a second embodiment of this invention.

The system LSI 10 according to the second embodiment has a substantially similar structure with the system LSI according to the first embodiment.

However, the second embodiment is different from the first embodiment in that an organic substrate is used instead of the silicon substrate 11.

Herein, it is to be noted that organic material, such as, epoxy resin and polyimide, is used as a base member. As the organic substrate, a flexible substrate having a relatively thin thickness and flexibility is suitable.

Subsequently, description will be made about a method of manufacturing the system LSI 10 according to the second embodiment.

Referring to Figs. 8A through 8E, description will be made about a method of manufacturing a global wiring layer 8 of the system LSI 10.

A plurality of second wiring layers 20 a are laminated by the use of the known forming method of the multiple wiring pattern to form the second wiring layer 20, as shown in Fig. 8A.

Successively, the global wiring layer 8 is manufactured in the same manner as the steps illustrated in Figs. 5A through 5E, as shown in Figs. 8B through 8E.

Referring to Figs. 9A through 9C, description will be made about a method of manufacturing the system LSI 10 according to the second embodiment.

In the system LSI cell portion 7, the functional blocks 2 to 6 are formed on the surface of the silicon chip 1 in the same steps illustrated in Figs. 4A through Fig. 4C

The global wiring layer 8 is transferred onto the system LSI cell portion 7 illustrated in Fig. 4C, as illustrated in Fig. 9A. In this event, the system LSI cell portion 7 is mounted on a stage (not shown) while the global wiring layer 8 is transferred on the condition that the global wiring layer 8 is turned over.

Under this circumstance, the pads 2a to 6a of the system LSI cell portion 7 are positioned in opposition to the wiring layer 15 of the global wiring layer 8 by using a position detecting device, such as, an image camera.

Next, the system LSI cell portion 7 and the global wiring layer are overlapped to each other. In the condition, a pressure is applied upwards and downward, and a heating process is carried out, as illustrated in Fig. 9B.

Thereby, the adhesive layer 16 is heat-hardened, and the system LSI cell portion 7 and the global wiring layer 8 are bonded and hardened.

Consequently, the pads 2a to 6a of the system LSI cell portion 7 are coupled with the second wiring layer 15 of the global wiring layer 8, and are mutually and electrically connected.

Finally, solder balls are supplied on the surface of the second wiring layer 20a exposed at an upper side of the global wiring layer 8, and are welded to for bumps 26. Thereby, the system LSI 10 is completed.

Thus, as the material of the global wiring layer 8, the organic substrate formed by the organic material is used instead of the silicon substrate 11 as the semiconductor substrate 11 of the first embodiment in the second embodiment.

Thereby, the second wiring layer 20, which electrically connects the functional blocks 2 to 6 with the bumps 26, is integrally formed with the global wiring layer 8.

In consequence, the physical strength is enhanced, and the electrical connection reliability is also enhanced. Further, a technique, which has a low cost and is generally utilized for the organic wiring substrate, is applicable.

(Third Embodiment)

Referring to Fig. 10, description will be made about a system LSI 10 according to a third embodiment of this invention.

The system LSI 10 according to the second embodiment has a substantially similar structure with the system LSI according to the first embodiment.

However, the third embodiment is different from the first embodiment in that the system LSI cell portion 7 is connected to the global wiring layer 8 with a space 31 through inner bumps 30.

Subsequently, description will be made about a method of manufacturing the system LSI 10 according to the third embodiment.

Referring to Figs. 11A through 11F, description will be made about a method of manufacturing a global wiring layer 8 of the system LSI 10 according to the third embodiment.

The global wiring layer 8 is manufactured in the same steps illustrated in Figs. 5A through 5E, as illustrated in Figs. 11A through 11 E.

Successively, the solder balls are supplied to specific portions of the surface of the second wiring layer 15 to form the inner bumps on the global wiring layer 8, as illustrated in Fig. 11F.

Referring to Figs. 12A through 12C, description will be made about a method of manufacturing the system LSI 10 according to the third embodiment.

First, the system LSI cell portion 7 has been completed in the same steps illustrated in Figs. 4A through Fig. 4C.

The global wiring layer 8 is transferred onto the system LSI cell portion 7 illustrated in Fig. 4C, as illustrated in Fig. 12A. In this event, the system LSI cell portion 7 is mounted on a stage (not shown) while the global wiring layer 8 is transferred on the condition that the global wiring layer 8 is turned over.

Under this circumstance, the pads 2a to 6a of the system LSI cell portion 7 are positioned in opposition to the second wiring layer 15 of the global wiring layer 8 by using a position detecting device, such as, an image camera.

Next, a pressure is applied upwards and downward for the system LSI cell portion 7 and the global wiring layer 8, and a heating process is carried out for them to melt the inner bumps 30, as illustrated in Fig. 12B.

Thereafter, a cooling process is performed, and the system LSI cell portion 7 and the global wiring layer 8 are connected to each other via the inner bumps 30 with the space 31, as shown in Fig. 12B.

Finally, the silicon substrate 11 is polished from an upper side of the

global wiring layer 8. Thereby, the buried vias 12 serving as the connection terminals with external circuit are exposed to the surface. Thus, the system LSI 10 is completed.

In the third embodiment, the system LSI cell portion 7 and the global wiring layer 8 are connected to each other via the inner bumps 30 such that the space 31 is formed therebetween.

Thereby, the global wiring layer 8 serving as dielectric is not adjacently and directly arranged for the system LSI cell portion 7.

Consequently, the system LSI cell portion 7 is readily and electrically separated from the global wiring layer 8, and the electrical characteristics for the high-frequency signal is improved. More specifically, transmission delay time becomes short.

When the physical characteristics is more important than the electrical characteristic, the space 31 may be sealed with filling material such as resin.

(Fourth Embodiment)

Referring to Fig. 13, description will be made about a system LSI 10 according to a fourth embodiment of this invention.

The system LSI 10 according to the forth embodiment combines the system LSI 10 of the second embodiment and the system LSI 10 of the third embodiment.

Subsequently, description will be made about a method of manufacturing the system LSI 10 according to the fourth embodiment.

The functional blocks 2 to 6 are formed on the surface of the silicon chip 1 in the same steps illustrated in Figs. 4A through Fig. 4C.

Referring to Figs. 14A through 14E, description will be made about a method of manufacturing the global wiring layer 8.

The second wiring layer 20 having the second wiring pattern 20a is formed in the same manner as the steps illustrated in Figs. 8A through 8D,

as shown in Figs. 14 A through 14D.

Subsequently, the inner bumps 30 for connecting the system LSI cell portion 7 are formed by supplying and melting the solder balls onto the second wiring layer 15, as illustrated in Fig 14E. Thereby, the global wiring layer 8 is manufactured.

Referring to Figs. 15A through 15C, description will be made about the system LSI 10 according to the fourth embodiment.

First, the system LSI cell portion 7 and the global wiring layer 8 are connected to each other in the same steps illustrated in Figs. 12A and 12B, as shown in Figs. 15A and 15B.

Finally, the bumps 26 are formed in the same steps illustrated in Fig. 9C, as shown in Fig. 15C. Thus, the system LSI 10 is completed.

Thus, as the material of the global wiring layer 8, the organic substrate formed by the organic material is used in lieu of the silicon substrate 11 as the semiconductor substrate of the first embodiment in the fourth embodiment.

Thereby, the second wiring layer 20, which electrically connects the functional blocks 2 to 6 with the bumps 26, is integrally formed with the global wiring layer 8.

In consequence, the physical strength is enhanced, and the electrical connection reliability is also enhanced. Further, a technique, which has a low cost and is generally utilized for the organic wiring substrate, is also applicable.

In addition, the system LSI cell portion 7 and the global wiring layer 8 are connected to each other via the inner bumps 30 such that the space 31 is formed therebetween.

Thereby, the global wiring layer 8 serving as dielectric is not adjacently and directly arranged for the system LSI cell portion 7.

Consequently, each impedance of the system LSI cell portion 7 and the global wiring layer 8 is lowered, and the electrical characteristic for the high-frequency signal is improved.

(Fifth Embodiment)

Referring to Fig. 16, description will be made about a method of manufacturing a system LSI 10 according to a fifth embodiment of this invention.

In the first through fourth embodiments, after the system LSI cell portion 7 is manufactured on the respective silicon chip 1 separated by dicing from the semiconductor wafer, the global wiring layer 8 manufactured from silicon substrate 11 having the same dimension as the silicon chip 1 is laminated.

By contrast, a plurality system LSI cell portions 7 are manufactured on the silicon wafer 101 before dicing in the fifth embodiment, as illustrated in Fig. 16A. Thereafter, a plurality global wiring layers 8 are manufactured on the silicon substrate 111, as illustrated in Fig. 16B.

After the silicon wafer 101 and the silicon substrate 101 are laminated, the silicon wafer 101 and the silicon substrate 111 are integrated and diced to separate the respective system LSIs, as illustrated in Fig. 16C.

More specifically, the sputtering process, the development and exposing process, and the patterning process are first performed onto the silicon wafer 101, and a plurality of system LSI cell portions 7 are arranged in a plan direction on the silicon wafer 101, as illustrated in Fig. 16A.

Subsequently, the first wiring layer 13, the insulating layer 14, the second wiring layer 15, and the adhesive layer 16 or the inner bump 30 are formed on the silicon substrate 111 in the same steps as the first through fourth embodiments, and thereby, a plurality of global wiring layers 8 are arranged in a plan direction, as illustrated in Fig. 16B.

Successively, the silicon substrate 111 is transferred and positioned onto the silicon wafer 101 on the condition that the silicon substrate 111 is turned over, as illustrated in Fig. 16C. Thereby, the silicon wafer 101 is in opposition to the silicon substrate 111.

Next, a pressure is applied upwards and downwards for the silicon wafer 101 and the silicon substrate 111 by the use of a pair of pressure applying and heating rollers 50 to laminate them, as shown in Fig. 16D.

Finally, the laminated silicon wafer 101 and the silicon substrate 111 are diced to separate into the respective system LSIs 10, as shown in Fig. 16E.

Thus, in the fourth embodiment, a plurality of system LSI cell portions 7 formed on the silicon wafer 101 and a plurality of global wiring layers 8 formed on the silicon substrate 111 are laminated to each other. Thereafter, the laminated silicon substrate 111 and the silicon wafer 101 are separated into the respective system LSI 10.

In the first through fourth embodiments, the silicon chip 1 and the silicon substrate 11 are exemplified, and the silicon wafer 101 and the silicon substrate 111 are exemplified in the fifth embodiment. However, the material is not restricted to the silicon, and a variety of semiconductor materials, such as, GaAs (gallium arsenide) may be used.

Although the bump 26 is formed on the global wiring layer 8 only in the second and fourth embodiments, the bump 26 may be formed on the exposed surface of the buried via 12 in the other embodiments.

In the third and fourth embodiments, the pads 2a to 6a are formed on the system LSI cell portion 7 while the second wiring layer 8 is formed on the global wiring layer 8. Conversely, the pads may be formed on the global wiring layer 8 while the pads or the bumps may be formed on the system LSI cell portion 7.

Although the adhesive layer 16 is supplied in the final step of the global wiring layer 8, the adhesive layer 16 may be supplied in an arbitrary step among a group of steps for laminating the system LSI cell portion 7 with the global wiring layer 8.

Further, the adhesive layer 16 or the inner bump 30 may be formed on the system LSI cell portion instead of the global wiring layer 8.

According to this invention, the manufacturing yield can be enhanced. This reason will be explained below.

Namely, after the system LSI cell portion having the functional blocks and the global wiring layer can be independently manufactured the system LSI can be readily fabricated only by laminating or combining them.

Further, the manufacturing duration can be shortened. The reason will be explained as follows.

That is, after the system LSI cell portion having the functional blocks and the global wiring layer can be independently manufactured the system LSI can be readily fabricated only by laminating them.

Moreover, the selective degree of freedom can be enhanced with respect to the manufacturing process and the material of the global wiring layer. This is because the global wiring layer can be independently manufactured and the mounting equipment becomes cheaper.

Further, the physical characteristics and the electrical characteristics are improved, and the manufacturing cost can be reduced. This is because a selective range of the manufacturing process and the material of the global wiring layer can be widened.

In addition, the electrical characteristics for the high-frequency signal can be improved. The reason will be described below.

Namely, the functional block is laminated with the global wiring layer by the use of the bump. Thereby, the space is formed between the functional block and the global wiring layer.

Consequently, the dielectric constant is reduced, and the high-frequency characteristic is improved. Further, an unnecessary electrical coupling is weakened.

WHAT IS CLAIMED IS:

1. A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other.

2. A system semiconductor device as claimed in claim 1, wherein:

a plurality of the system LSI cell portions are formed on a semiconductor wafer,

a plurality of the global wiring layers are formed on the semiconductor substrate, and

the semiconductor wafer and the semiconductor substrate are laminated, diced and separated to obtain a plurality of the system semiconductor devices.

3. A system semiconductor device claimed in claim 1, wherein:

the global wiring layer comprises;

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer, and

a second wiring layer and an adhesive layer formed on the insulating layer.

4. A system semiconductor device claimed in claim 1, wherein:

the global wiring layer comprises;

a first wiring layer formed on an organic substrate,

an insulating layer formed on the first wiring layer, and

a second wiring layer and an adhesive layer formed on the insulating layer.

5. A system semiconductor device as claimed in claim 1, wherein:

the global wiring layer comprises;

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer.

6. A system semiconductor device claimed in claim 1, wherein:

the global wiring layer comprises;

a first wiring layer formed on an organic substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer.

7. A system semiconductor device as claimed in claim 3, wherein;

the insulating layer includes a via which electrically connects the first wiring layer with the second wiring layer.

8. A system semiconductor device as claimed in claim 1, wherein:

the global wiring layer has bumps for electrically connecting to an external circuit on a surface thereof.

9. A system semiconductor device as claimed in claim 1, wherein:

the global wiring layer includes buried vias which electrically connect the functional blocks to an external circuit.

10. A system semiconductor device as claimed in claim 1, wherein:

the global wiring layer has at least one or more of the wiring layers.

11. A system semiconductor device as claimed in claim 3, wherein:

the global wiring layer has at least one or more of the insulating layers.

12. A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which are serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that the functional blocks are electrically connected to each other.

13. A method as claimed in claim 12, wherein:

forming a plurality of the system LSI cell portions on a semiconductor wafer,

forming a plurality of the global wiring layers on the semiconductor substrate,

laminating the semiconductor wafer and the semiconductor substrate, and

dicing and separating the laminated semiconductor wafer and the semiconductor substrate to obtain a plurality of the system semiconductor devices.

14 . A method as claimed in claim 12, wherein:

the global wiring layer is formed by sequentially laminating a first wiring, an insulating layer, a second wiring layer, and an adhesive layer on the semiconductor substrate.

15. A method as claimed in claim 12, wherein:

the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer ,and an adhesive layer on an organic substrate.

16. A method as claimed in claim 12, wherein:

the global wiring layer is formed by sequentially laminating a first

wiring layer, a second wiring layer, an insulating layer, and inner bumps on the semiconductor substrate .

17. A method as claimed in claim 12, wherein:

the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer, and inner bumps on an organic substrate.

18. A method as claimed in claim 14, further comprising the following step:

forming a via for electrically connecting the first wiring layer with the second wiring layer in the insulating film.

19. A method as claimed in claim 12, further comprising the following step:

forming bumps for electrically connecting to an external circuit on the global wiring layer.

20. A method as claimed in claim 12, further comprising the following step:

forming buried vias for electrically connecting the functional blocks to an external circuit in the global wiring layer .

21. A method as claimed in claim 12, further comprising the following step:

forming at least one or more of the wiring layers in the global wiring layer .

22. A method as claimed in claim 14, further comprising the following step:

forming at least one or more of the insulating layers in the global wiring layer.

Abstract of the Disclosure:

A system semiconductor device includes a system LSI cell portion and a global wiring layer. The system LSI cell portion has a plurality of functional blocks for realizing specific functions on a semiconductor chip. The global wiring layer has a wiring layer on a semiconductor substrate. The system LSI cell portion is laminated with the global wiring layer.

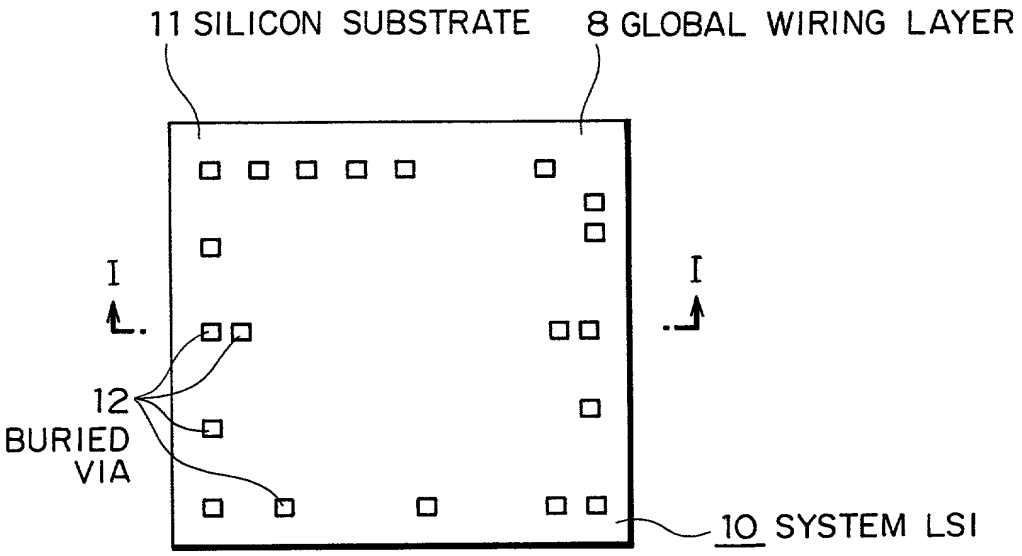

FIG. 1A

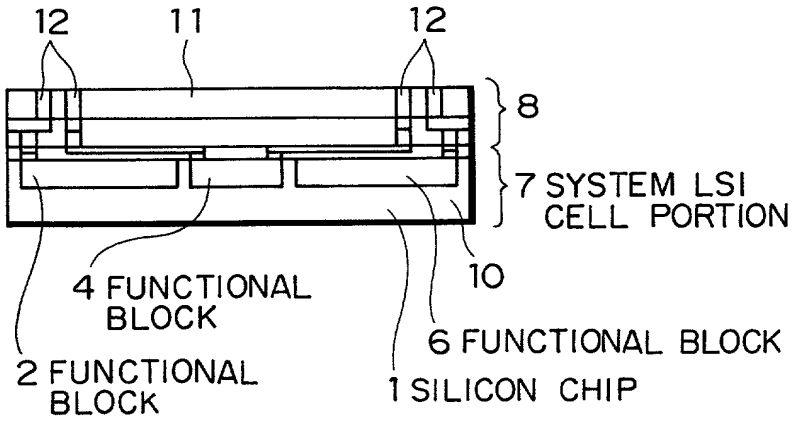

FIG. 1B

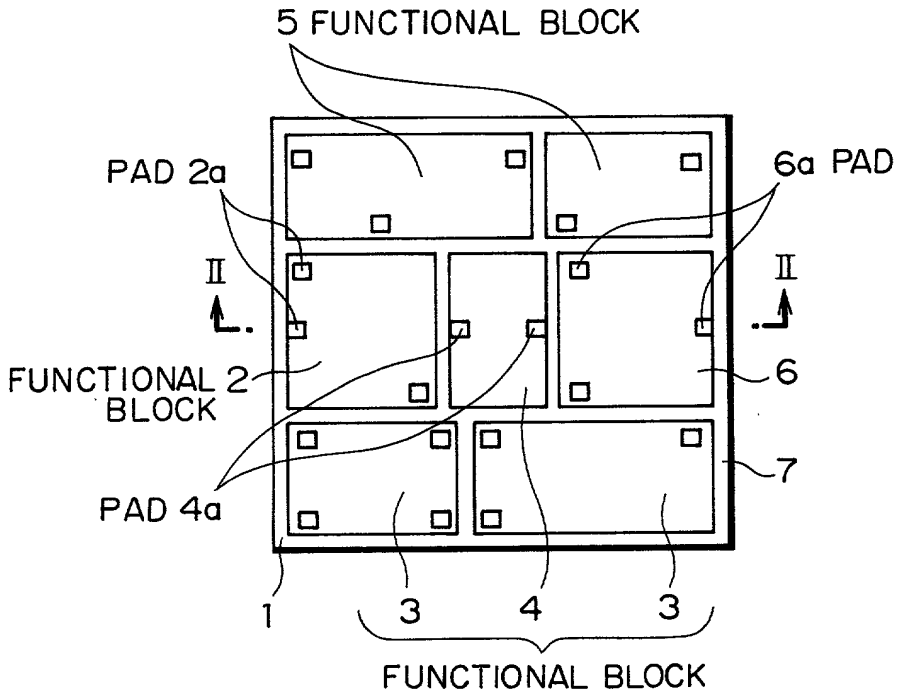
5 FUNCTIONAL BLOCK
PAD 2a
6a PAD
II
II
FUNCTIONAL 2
BLOCK
6
7
PAD 4a
1
3
4
3
FUNCTIONAL BLOCK

FIG. 2A

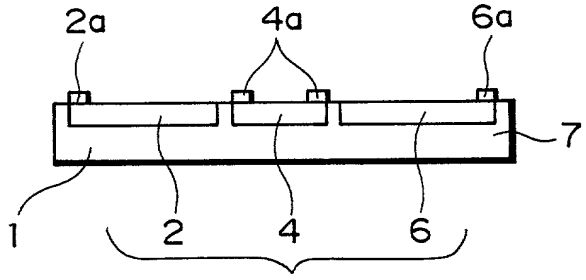
2a
4a
6a
7
1
2
4
6

FIG. 2B

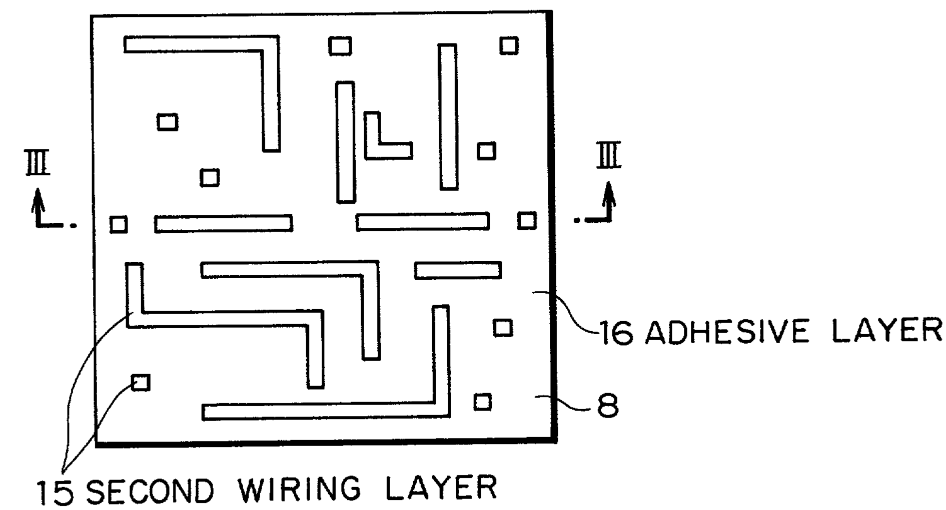
III
III
16 ADHESIVE LAYER
8
15 SECOND WIRING LAYER

FIG. 3A

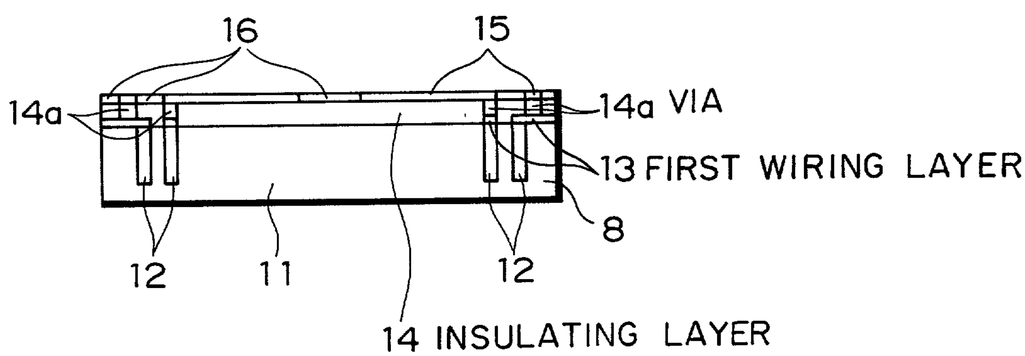
16
15
14a
14a VIA
13 FIRST WIRING LAYER
8
12
11
12
14 INSULATING LAYER

FIG. 3B

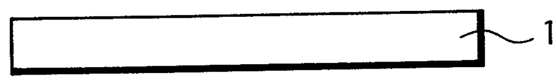

FIG. 4A

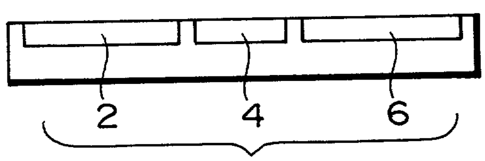

FIG. 4B

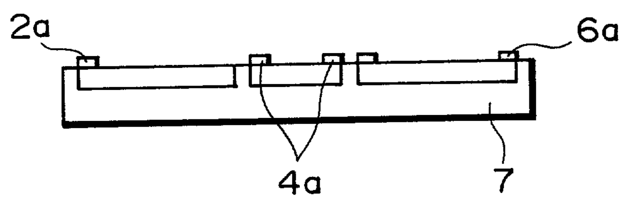

FIG. 4C

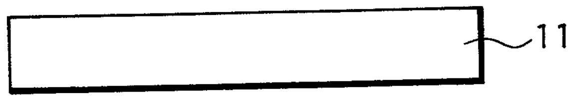

FIG. 5A

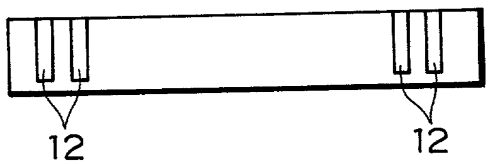

FIG. 5B

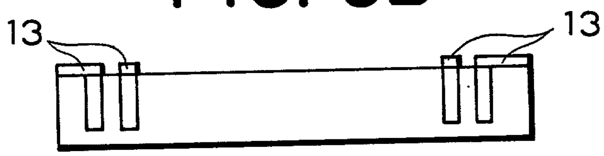

FIG. 5C

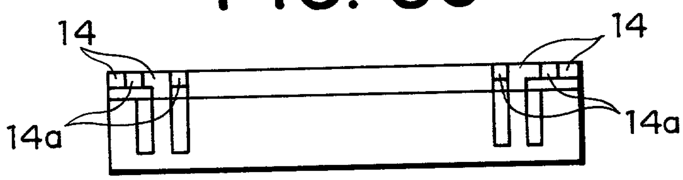

FIG. 5D

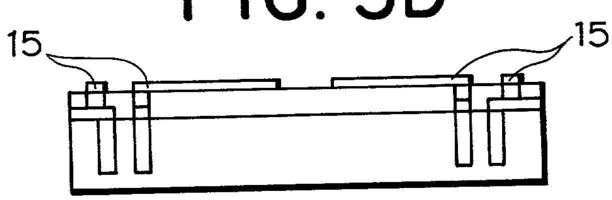

FIG. 5E

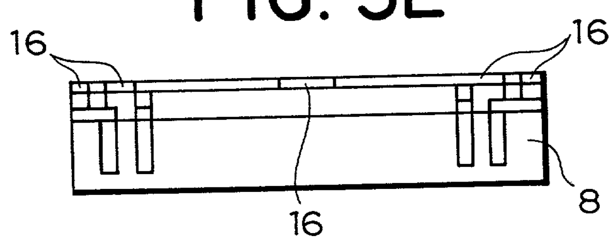

FIG. 5F

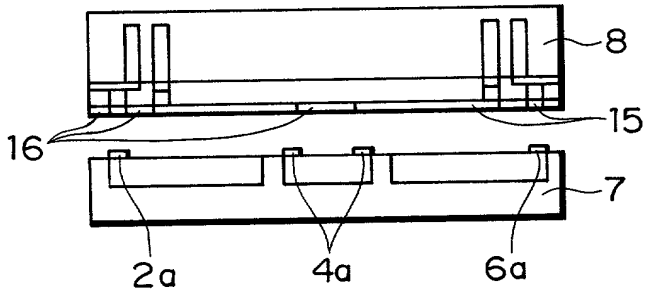

FIG. 6A

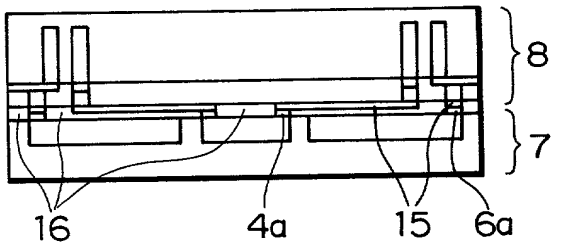

FIG. 6B

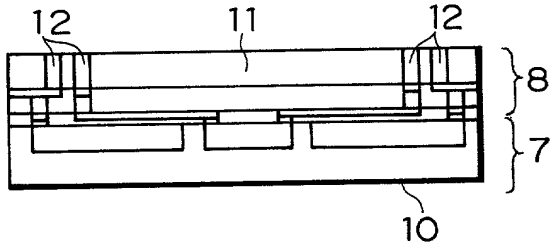

FIG. 6C

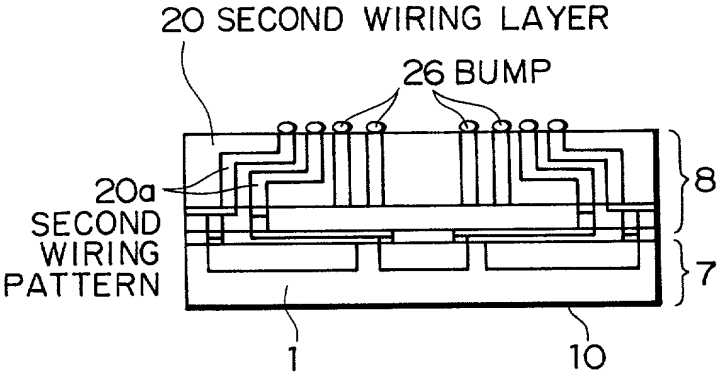

FIG. 7

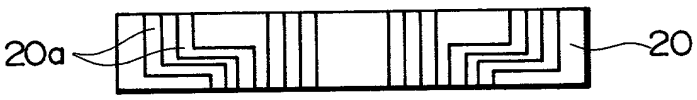

FIG. 8A

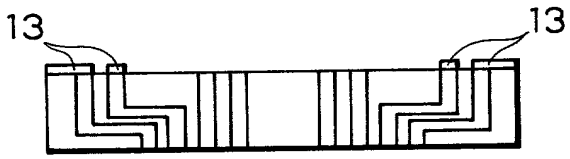

FIG. 8B

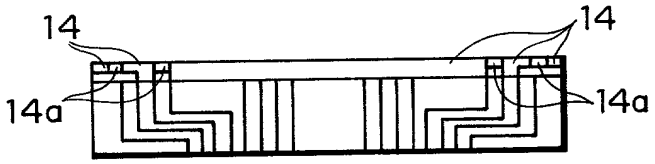

FIG. 8C

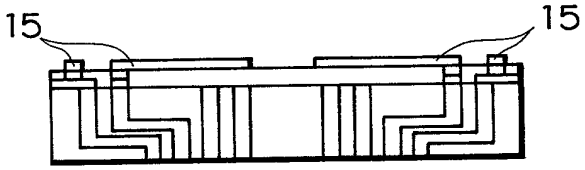

FIG. 8D

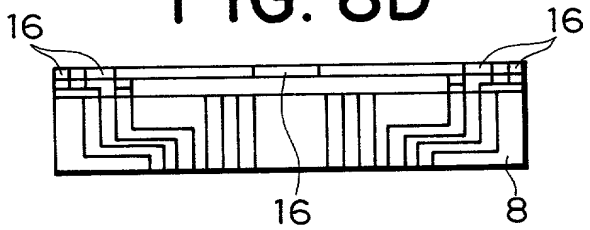

FIG. 8E

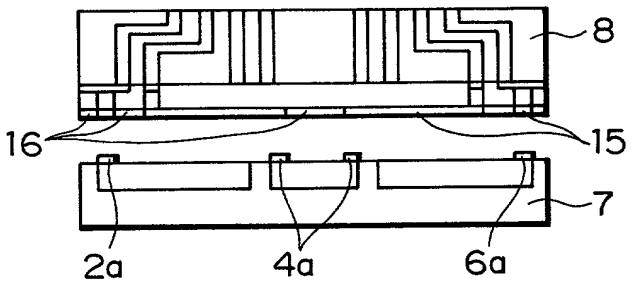

FIG. 9A

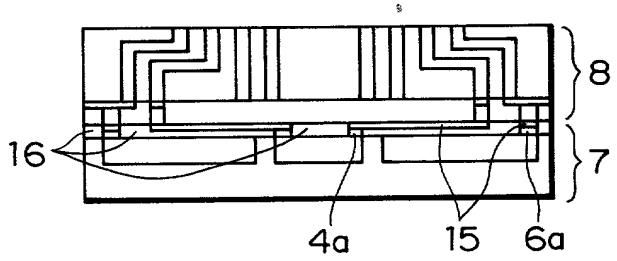

FIG. 9B

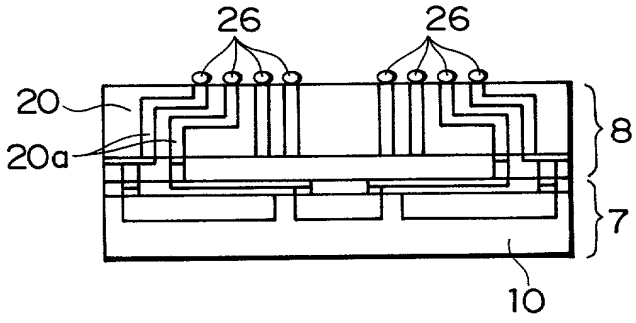

FIG. 9C

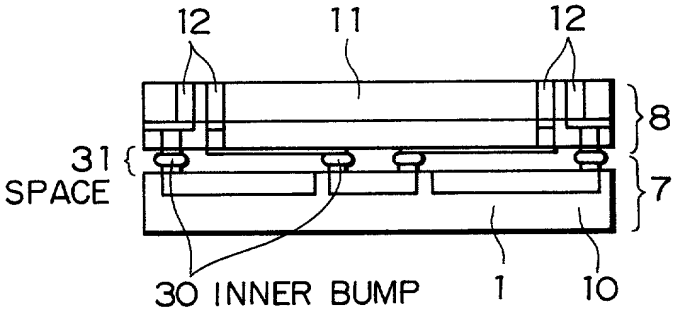

FIG. 10

FIG. 11A

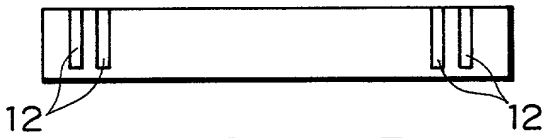

FIG. 11B

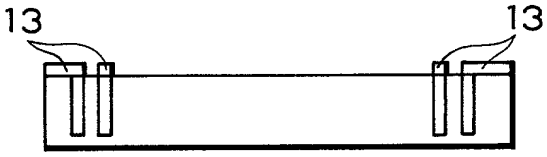

FIG. 11C

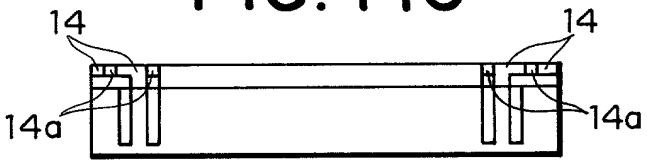

FIG. 11D

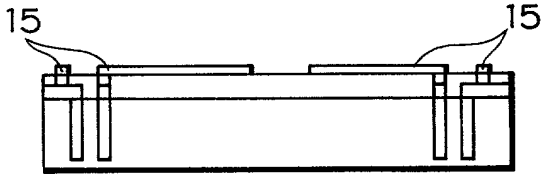

FIG. 11E

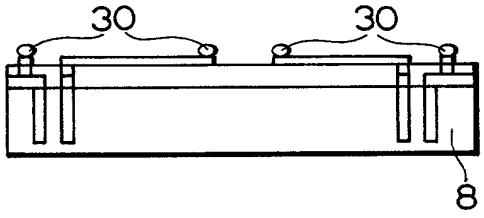

FIG. 11F

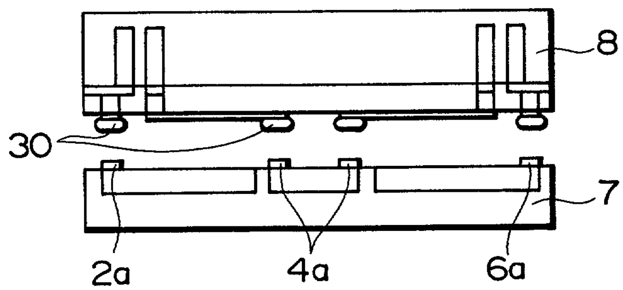

FIG. 12A

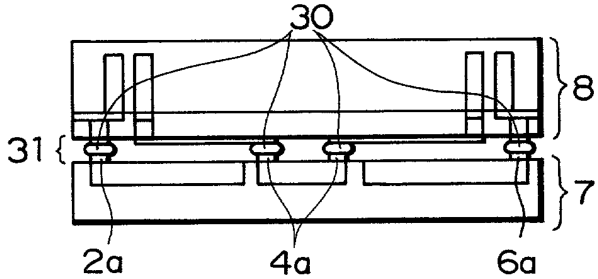

FIG. 12B

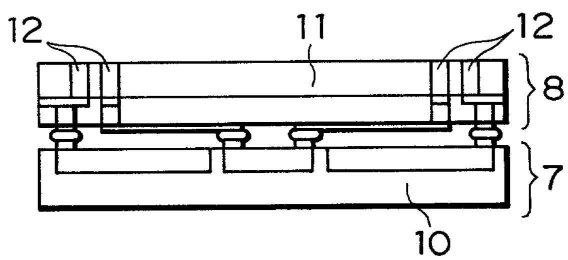

FIG. 12C

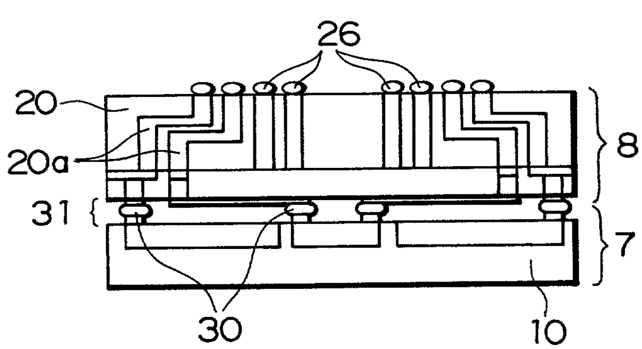

FIG. 13

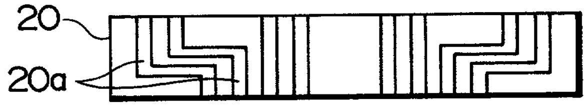

FIG. 14A

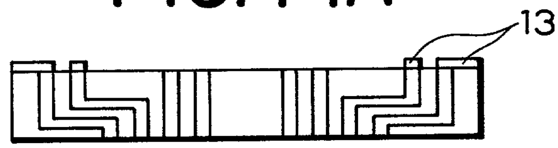

FIG. 14B

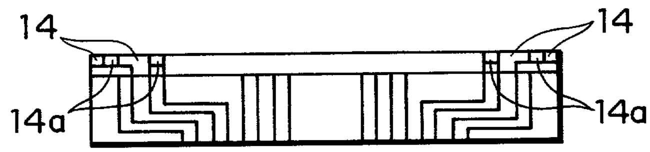

FIG. 14C

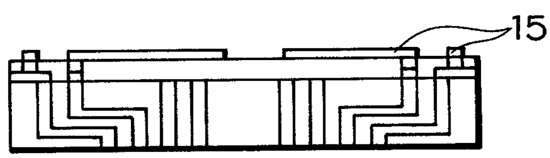

FIG. 14D

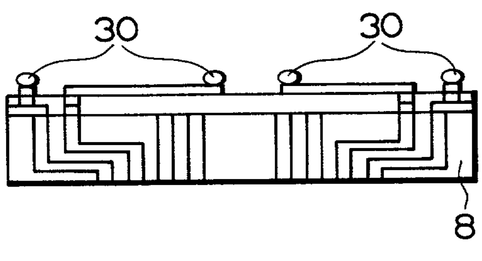

FIG. 14E

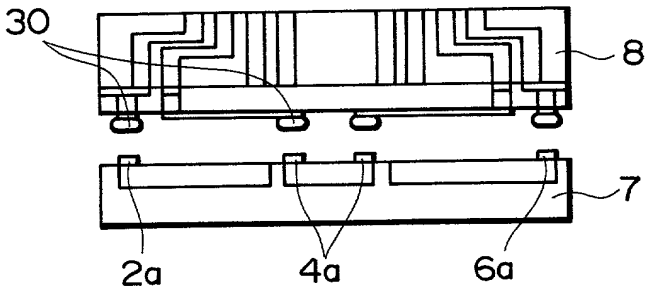

FIG. 15A

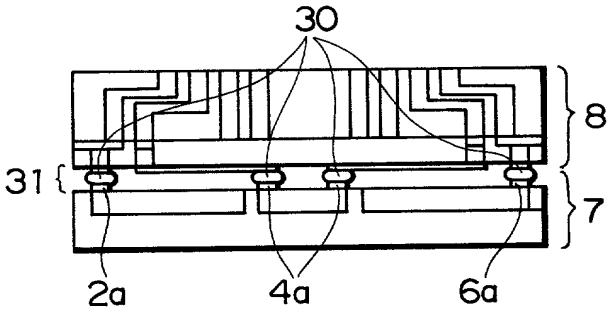

FIG. 15B

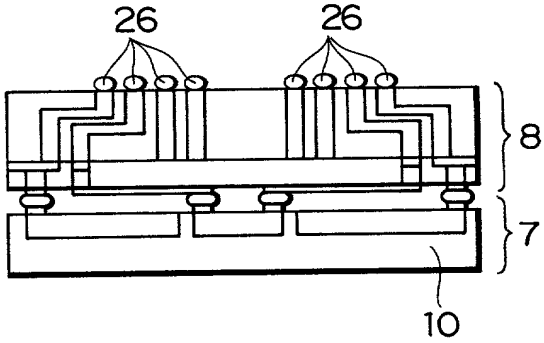

FIG. 15C

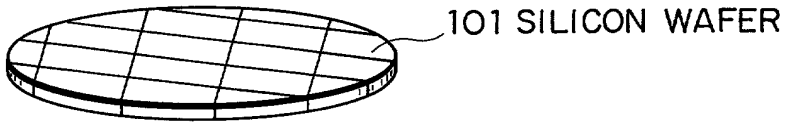

FIG. 16A

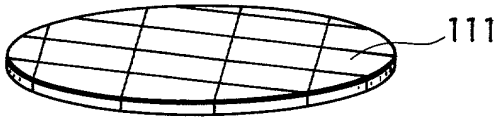

FIG. 16B

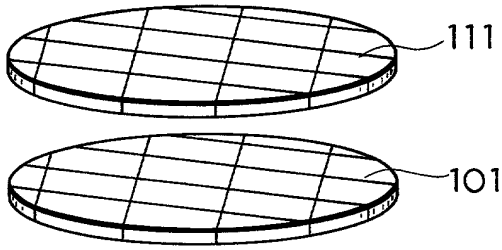

FIG. 16C

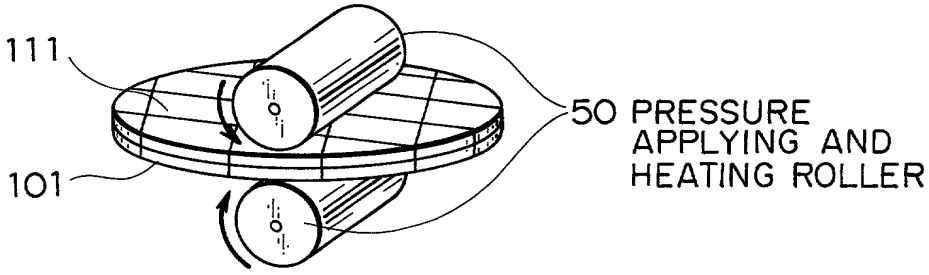

FIG. 16D

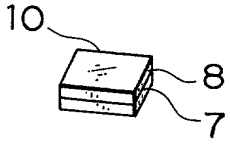

FIG. 16E

WN-2205
11-193962
Ref. ___________

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SYSTEM SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

the specification of which: *(check one)*

REGULAR OR DESIGN APPLICATION

[x] is attached hereto.

[ ] was filed on __________ as application Serial No. __________ and was amended on __________ (if applicable).

PCT FILED APPLICATION ENTERING NATIONAL STAGE

[ ] was described and claimed in International application No. __________ filed on __________ and as amended on __________ (if any).

09/631950

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

PRIORITY CLAIM

I hereby claim foreign priority benefits under 35 USC 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)

Country	Application Number	Date of Filing (day, month, year)	Priority Claimed
Japan	193962/1999	8/7/1999	yes

(Complete this part only if this is a continuing application.)

I hereby claim the benefit under 35 USC 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Filing Date) (Status--patented, pending, abandoned)

POWER OF ATTORNEY

The undersigned hereby authorizes the U.S. attorney or agent named herein to accept and follow instructions from ____________________________ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorney or agent named herein will be so notified by the undersigned.

As a named inventor, I hereby appoint the following attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: **Robert J. PATCH, Reg. No. 17,355, Andrew J. PATCH, Reg. No. 32,925, Robert F. HARGEST, Reg. No. 25,590, Benoît CASTEL, Reg. No. 35,041, Eric JENSEN, Reg. No. 37,855, and Thomas W. PERKINS, Reg. No. 33,027**, c/o YOUNG & THOMPSON, Second Floor, 745 South 23rd Street, Arlington, Virginia 22202.

Address all telephone calls to Young & Thompson at 703/521-2297.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

09614337.070700

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Inventor's signature ____________________ Date ____________

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